Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-4. (Canceled)

5. (Currently amended) An active matrix pixel device comprising a plurality of polycrystalline silicon islands supported by a substrate, one of the polycrystalline silicon islands providing a channel and doped source/drain regions of a thin film transistor, the active matrix pixel device further comprising a PIN diode which includes a p-type doped region and an n-type doped region separated by an amorphous silicon intrinsic region, wherein the amorphous silicon intrinsic region overlies and contacts at least a part of one of the polycrystalline silicon islands which provides one of the p-type or n-type doped regions of the PIN diode, wherein the doped source/drain regions and said one of the p-type or n-type doped regions of the PIN diode are provided by the same polycrystalline silicon island and a vertical n-i-p stack is used by using a doped region of ~~the~~ a polysilicon thin film transistor

(TFT) for the n-type doped region.

6. (Canceled)

7. (Currently amended) An active matrix pixel device comprising a plurality of polycrystalline silicon islands supported by a substrate, one of the polycrystalline silicon islands providing a channel and doped source/drain regions of a thin film transistor, the active matrix pixel device further comprising a PIN diode which includes a p-type doped region and an n-type doped region separated by an amorphous silicon intrinsic region, wherein the amorphous silicon intrinsic region overlies and contacts at least a part of one of the polycrystalline silicon islands which provides one of the p-type or n-type doped regions of the PIN diode, wherein both the p-type and n-type doped regions of the PIN diode are provided by respective ones of the polycrystalline silicon islands, and wherein a distance between the p-type and n-type doped regions is substantially equal to a gap between adjacent thin film transistors (TFTs).

8. (Previously presented) An active matrix pixel device according to claim 7, further comprising a second thin film transistor having doped source/drain regions provided by one of the polycrystalline silicon islands, the doped source/drain regions being of an opposite conductivity type to those of a first thin film transistor, wherein the n-type doped region of the PIN diode is provided by a doped source/drain region of one transistor and the p-type doped region of the PIN diode is provided by a doped source/drain region of the other transistor.

9. (Currently amended) An active matrix pixel device according to claim 7, wherein a transparent conductive gate overlies the amorphous silicon intrinsic region of the PIN diode separated therefrom by an insulating layer, the gate serving to apply a voltage to the intrinsic region so as to control ~~the~~ a conductivity between the n-type and p-type doped regions.

10. (Previously presented) An active matrix pixel device according to claim 5, wherein the thin film transistor further comprises a gate electrode which serves to control a current through the channel, and wherein the amorphous silicon intrinsic

region of the PIN diode overlies the gate electrode.

11. (Previously presented) An active matrix electroluminescent display device according to claim 5, wherein the PIN diode serves to measure a light intensity output from an associated display element and supply a signal to drive circuitry connected thereto to enable modulation of the light intensity output in accordance with the measured light intensity output.